WHAT IS CLAIMED IS:

1. A digital decoding system for demodulating a modulated analog signal containing a L+R signal, a L-R signal centered around a carrier signal, and a pilot signal, the system comprising:

an analog to digital converter adapted to convert the analog signal into a digital signal;

first, second, and third digital filters adapted to separate the L+R signal, the pilot signal, and the L-R signal, respectively, from the digital signal;

clock reconstitution circuitry adapted to reconstitute a clock signal from the pilot signal;

L-R signal recovery circuitry adapted to recover the L-R signal using the reconstituted clock signal; and

channel recovery circuitry adapted to recover a left channel signal and a right channel signal from the L+R signal and the L-R signal.

2. The digital decoding system of claim 1 wherein the first digital filter is a low pass filter, the second digital filter is a bandpass filter, and the third digital filter is a high pass filter.

3. The digital decoding system of claim 2 wherein the low pass filter has a cut-off frequency of approximately 13.8 kHz, the band pass filter is centered at approximately 15.734 kHz, and the high pass filter is adapted to remove frequencies that pass through the low pass and band pass filters.

4. The digital decoding system of claim 2 further comprising additional signal recovery circuitry including a demodulator adapted to receive input from the clock reconstitution circuitry and the high pass filter, wherein the additional signal recovery circuitry is adapted to recover a signal other than the L+R signal, L-R signal, and pilot signal from the modulated analog signal.

5. The digital decoding system of claim 4 wherein the additional signal is a second audio program (SAP) signal.

6. The digital decoding system of claim 2 wherein the L-R signal recovery circuitry includes:

a synchronous demodulator adapted to demodulate the L-R signal received from the high pass filter using clock information from the clock reconstitution circuitry; and

an expander for expanding the demodulated L-R signal.

7. The digital decoding system of claim 1 wherein the clock reconstitution circuitry comprises a phase-locked loop (PLL) associated with at least one lookup table.

8. The digital decoding system of claim 7 wherein an output of the PLL represents a phase of the pilot signal, and wherein the output is used to address the lookup table to generate a sine wave for the L-R signal recovery circuitry.

9. The digital decoding system of claim 7 wherein the PLL comprises a digital phase accumulator and a second order accumulator.

10. The digital decoding system of claim 7 wherein the PLL includes a sample rate of approximately 24 MHz.

11. The digital decoding system of claim 1 wherein the channel recovery circuitry is adapted to calculate a sum and a difference of the L+R signal and the L-R signal.

12. The digital decoding system of claim 1 further comprising a digital to analog converter adapted to convert the recovered left channel and right channel signals from digital signals into analog signals.

13. A demodulator for digitally demodulating a received analog signal including having a pilot signal, a L+R signal, and a L-R signal, the demodulator comprising:

an analog to digital converter for converting the received analog signal to a digital signal;

a plurality of filters for separating the pilot signal, L+R signal, and L-R signal into a clock reconstitution path, a L+R signal path, and a L-R signal path, respectively;

circuitry within the clock reconstitution path for reconstituting a clock signal from the pilot signal;

circuitry within at least one of the L+R and L-R signal paths for recovering at least one of the L+R or L-R signals using the reconstituted clock signal; and

circuitry for recovering a Left signal and a Right signal from the L+R signal path and the L-R signal path.

14. The demodulator of claim 13 wherein the circuitry for recovering the Left and Right signals includes a demultiplexing matrix.

15. The demodulator of claim 13 wherein the circuitry within the clock reconstitution path includes a phase-locked loop (PLL) associated with at least a first lookup table, wherein the PLL is adapted to generate a digital value that is compared to a plurality of digital values in the first lookup table for use in at least one of the L+R and L-R signal paths.

16. The demodulator of claim 15 further comprising additional signal recovery circuitry adapted to recover a signal other than the L+R signal, L-R signal, and pilot signal.

17. The demodulator of claim 16 wherein the circuitry within the clock reconstitution path includes a second lookup table for use with the additional signal recovery circuitry.

18. A method for digitally decoding an encoded signal, the method comprising:

receiving an encoded signal from a single analog channel, wherein the encoded signal includes at least first and second audio signals;

performing an analog to digital conversion on the received signal;

separating the converted signal using multiple digital filters into first and second signal paths for the first and second audio signals, respectively, and a clock reconstitution path; and

recovering the first and second audio signals using the first and second signal paths,

respectively, wherein at least one of the first and second audio signals is recovered based on information from the clock reconstitution path.

19. The method of claim 18 further comprising performing a digital to analog conversion on the two recovered audio signals.

20. The method of claim 18 wherein recovering at least one of the first and second audio signals includes reconstituting clock information carried within the received signal.